REMARKS/ARGUMENTS

After the foregoing Amendment, claims 1-20 are currently pending in this application. Claims 5-10 and 15-16 have been withdrawn. Claims 1, 4, 11, 13, and 20 have been amended to recite that the system performance parameter to be optimized is selected from a group consisting of latency, bandwidth, and safety; and/or that the data source from which data is received at the data input is one of a link input and a memory. Support is found at least in paragraphs **[0010]**, **[0012]**, **[0017]**, **[0018]**, and **[0022]**.

In the specification, a new title has been provided, as suggested by the Examiner.

Applicants submit that no new matter has been introduced into the application by these amendments.

Regarding Examiner's Response to Arguments

In paragraph 3 of the Office Action, the Examiner contends that Applicants have failed to distinguish between the teachings of the references and the claims, and that Applicants' arguments are largely conclusory statements about the reference that fail to address what the Examiner contends is language analogous to the claims. Applicants disagree. On the contrary, Applicants have clearly and specifically distinguished the claims from the references. For example, regarding *Sprangle*, Applicants asserted "the memory access mode changes in *Sprangle* affect only the fetching of data from memory ... and do not affect the delivery of data from an input to an output ... while the data is in transit... In contrast, the mode changes of the claimed invention affect the delivery of data ... while the data is in transit, but have nothing to do with fetching data from memory. Indeed, in the claimed invention the data need not even be received from memory..." (emphasis added).

In addition, the Examiner refers to "paragraph 6, and claims 1, 5, 6, 10, and 11," apparently of *Sprangle*, as containing clear teachings analogous to the claims. Applicants disagree. The Examiner has not recited the specific language contended to be analogous to the claims, and Applicants are not able to find such analogous language in the locations cited. For example, the cited locations of *Sprangle* refer to predicting open memory pages, and switching memory access modes in accordance with those predictions to minimize memory access latency or maximize memory bus bandwidth. However, *Sprangle* does not mention performing operations on data in transit from a data input to a data output. In contrast, in the claims it is not relevant which memory pages are open, neither is it relevant in which mode memory is accessed. In fact, as noted above, data in transit from the data input to the data output need not even have been obtained from memory.

Regarding paragraph 4, the Examiner's comments regarding Applicant's alleged assertion that *Sprangle* teaches away is not understood, because Applicants made no such assertion. Applicants simply asserted that *Sprangle* solves an unrelated problem in an unrelated way.

Regarding paragraph 6, the Examiner argues that the individual references and not the combinations were attacked, contending that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. The Examiner might not have appreciated Applicants' arguments that the elements alleged by the Examiner to be found in the cited references do not actually exist in those references. To establish a *prima facie* case for obviousness, it must be shown that the asserted references teach all of the elements of the examined claims. If all of the elements cannot be found in the

references in any possible combination, then arguing against their combination is irrelevant. Elements that are not present cannot be combined.

Objections to the Specification

The specification is objected to as allegedly failing to provide proper antecedent basis for the claimed subject matter. In particular, the Examiner contends there is no teaching in the specification of data being "in transit to the data output from any source." The claims have been amended to recite that the data received at the data input is from a source from the group consisting of a link input (**18**) and a memory (**24**), as disclosed in paragraphs **[0010]** and **[0012]**, respectively, and shown in Fig. 1.

The Examiner also objected to the title as allegedly not being descriptive. A new title has been provided to overcome the objection.

Withdrawal of the objections to the specification is respectfully requested.

Claim Rejections - 35 USC § 112

Claims 1-4, 11-14, and 17-20 stand rejected under 35 USC § 112 second paragraph as allegedly being indefinite, because it is unclear how the claimed systems are able to receive and transmit from any source. The claims have been amended to claim that the data source is from the group consisting of a link input and a memory. Withdrawal of the 35 USC § 112 rejection of these claims is respectfully requested.

Claim Rejections - 35 USC § 102

Claims 1-4 and 17 stand rejected under 35 USC § 102(a) as being allegedly anticipated by U.S. Patent Application Publication 2003/0159008 to *Sprangle* et al. (hereinafter "*Sprangle*"). Applicants respectfully traverse this rejection.

The claims recite methods and apparatus for delivering data from a data input to a data output within a data processing system, and include selecting a system performance parameter to be optimized from the group consisting of latency, bandwidth, and safety; and receiving at the data input a sequence of discrete data words in transit to the data output from a source from the group consisting of a link input and a memory.

It is well settled that a reference must teach every element or aspect of a claim in order to anticipate the claim under 35 USC § 102(a). However, *Sprangle* does not do so.

Sprangle discloses a method and apparatus for controlling access to memory, comprising monitoring memory access requests from a hardware prefetcher and an out-of-order processor core, determining whether the memory accesses from the hardware prefetcher are used by the out-of-order core, and switching memory accesses from a first mode to a second mode depending on the percentage of memory accesses generated by the hardware prefetcher that are actually used by the out-of-order core.

The memory access mode changes in *Sprangle* affect only the timing of accessing data in memory for use by an out-of-order processor core, and are not concerned with the timing or sequence of delivery of data words from an input to an output, such as the data fetched from the memory for the processor, while the data is in transit from the input to the output. After the data is fetched from memory in *Sprangle*, the data is delivered from the memory to the processor without regard to its sequence or timing. In contrast, the mode changes of the claimed invention do indeed affect the delivery of data while the data is in transit. However, the mode changes have nothing to do with fetching data from memory. Indeed, in the claimed invention the data need not even have been fetched at all, nor must it come from a memory. Instead, the data can

be received from a link input and not from a memory, and the data can be received without having been fetched. For example, data received from a link input may be from a network link, may have been sent from another computer, and may be unanticipated. In addition, *Sprangle* discloses fetching memory only so as to minimize latency or maximize bandwidth. In contrast, the claimed invention delivers data so that safety can also be optimized.

Notably, the claimed invention and *Sprangle* may both be advantageously used independently in the same computer, even if the source of the data is a memory. For example, in a system having an out-of-order processor core, but in which a connection from the DRAM to the CPU is unreliable, *Sprangle* can be used to minimize memory access latency in fetching data from memory, while the claimed invention can be used to maximize the data delivery safety of the same data transaction.

With regard to claim 1, the Examiner asserts that *Sprangle* teaches receiving at a data input a sequence of discrete data words, determining an optimum mode of delivery of the data words to the data output, and delivering the data words from the data input to the data output in the determined optimum mode. This is incorrect. As noted above, *Sprangle* discloses fetching data in a determined memory access mode, but does not disclose delivering data in a determined data delivery mode.

With regard to claim 4, the Examiner asserts that *Sprangle* teaches receiving a sequence of discrete data words in transit to a data output, and determining an optimum sequence and time of delivery of data words to the data output so as to optimize a selected performance parameter, citing paragraphs 16 and 22. This is incorrect. *Sprangle* therein discloses scheduling memory accesses by a FSB scheduler. However, it is only after the data in memory has been accessed that it is in transit. *Sprangle* is concerned only with scheduling data access, and cannot operate on data after it has been fetched and is in transit. In contrast, the claimed invention does indeed operate on data in transit from an input to an output. In addition, as noted above, *Sprangle*

discloses scheduling memory accesses only so as to minimize latency or maximize bandwidth. In contrast, the claimed invention delivers data so that safety can also be optimized.

Based on the arguments presented above, it can be seen that *Sprangle* does not teach all of the elements of claims 1 and 4. Because *Sprangle* does not teach all of the elements of claims 1 and 4, *Sprangle* cannot anticipate those claims under 35 USC § 102(a), and claims 1 and 4 are allowable over *Sprangle*. Claims 2, 3, and 17-20 depend from claim 1. Therefore, without prejudice to their individual merits, those claims are also allowable.

Based on the arguments presented above, withdrawal of the 35 USC § 102(a) rejection of claims 1-4 and 17 is respectfully requested.

Claims 11-14 stand rejected under 35 USC § 102(e) as being allegedly anticipated by U.S. Patent Application Publication 2004/0090924 to *Giaimo* et al. (hereinafter "*Giaimo*"). Applicants respectfully traverse this rejection.

Regarding claims 11 and 13, *Giaimo* does not disclose or suggest selecting a system performance parameter to be optimized from the group consisting of latency, bandwidth, and safety. In addition, *Giaimo* does not disclose or suggest receiving data from a source from the group consisting of a link input and a memory.

Because *Giaimo* does not teach all of the elements of claims 11 and 13, they are allowable over *Giaimo*. Claim 12 depends from claim 11, and claim 14 depends from claim 13. Therefore, without prejudice to their own individual merits, claims 12 and 14 are also allowable.

Based on the arguments presented above, withdrawal of the 35 USC § 102(e) rejection of claims 11-14 is respectfully requested.

Claim Rejections - 35 USC § 103(a)

Claims 18 and 19 are rejected under 35 USC § 103(a) as being allegedly unpatentable over *Sprangle* (same as above) in view of U.S. Patent 6,912,598 to *Bedarida*, et al. (hereinafter

"*Bedarida*"). Claim 20 is rejected under 35 USC § 103(a) as being allegedly unpatentable over *Sprangle* (same as above) in view of U.S. Patent Application Publication 2002/0018395 to *McLaury* (hereinafter "*McLaury*"). Applicants respectfully traverse these rejections.

To establish a *prima facie* case for obviousness under 35 USC § 103(a), it must be shown that the asserted references, when read alone or in combination, teach all of the elements of the examined claims. Also, a motivation to combine the references may be shown if more than one reference is being asserted, *KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, slip opinion 04-1350 at 15 (April 30, 2007).

Furthermore, the factual inquiries set forth in *Graham v. John Deere*, 383 U.S. 1 (1966), are applied for establishing a background for determining obviousness under 35 USC § 103(a). Those inquiries are: determining the scope and contents of the prior art; ascertaining the differences between the prior art and the claims at issue; resolving the level of ordinary skill in the pertinent art; and considering objective evidence present in the application indicating obviousness or non-obviousness.

Claims 18 and 19 depend from claim 1, and it is noted that *Bedarida* is relied on only for the additional features of claims 18 and 19. Therefore, without prejudice to their own individual merits, claims 18 and 19 are deemed allowable for at least the same reasons claim 1 is allowable.

Claim 20 depends from claim 1, and it is noted that *McLaury* is relied on only for the additional features of claim 20. Without prejudice to its own individual merits, claim 20 is deemed allowable for at least the same reasons claim 1 is allowable.

In addition, *McLaury* does not disclose or suggest a data storage element intermediate a data input and a data output for storing individual data words in transit from the data input to the data output for a determined time before delivery to the data output, as does claim 20. For this reason also, claim 20 is allowable over *McLaury*.

Based on the arguments presented above, withdrawal of the 35 USC § 103(a) rejection of claims 18-20 is respectfully requested.

Conclusion

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application, including claims 1-20, is in condition for allowance and a notice of allowance is respectfully requested.

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

Respectfully submitted,

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